

1. A variable width memory system comprising:
 - a bus for communicating information;
 - a plurality of memory locations coupled to said bus, said plurality of memory locations store information and bit widths of at least two of said memory locations are different; and
 - a controller coupled to said bus, said controller directs access to said plurality of memory locations.

2. The variable width memory system of Claim 1 wherein said plurality of memory locations are included on a single memory substrate.

3. The variable width memory system of Claim 1, wherein said plurality of memory locations are included in a random access memory (RAM).

4. The variable width memory system of Claim 1, wherein each one of said plurality of memory locations is identified by a unique internal identifier which is referenced by said controller to access said each one of said plurality of memory locations.

5. The variable width memory system of Claim 4, wherein said controller maps said unique internal identifier to a particular external indicator, wherein components referred to by said unique internal identifier and said particular external indicator have the same bit width.

6. The variable width memory system of Claim 1, wherein the bit width of at least two of said plurality of memory locations is the same.

7. The variable width memory system of Claim 1, wherein the bit width of at least one of said plurality of memory locations is configured in accordance with criteria directed at decreasing processor operations.

8. A variable width memory mapping method comprising:

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receiving a register indicator corresponding to a register;
 accessing a memory cell based on said register indicator, wherein said
 memory cell and said register have same bit capacity; and
 transferring information between said memory cell and another
 5 component, wherein said information includes the same number of bits as
 said bit capacity.

9. The variable width memory mapping method of Claim 8 wherein
 said register indicator is received from a processor.

10. The variable width memory mapping method of Claim 8 wherein
 said bit capacity is determined by processing criteria associated with a
 processor.

11. The variable width memory mapping method of Claim 8 wherein
 said information is part of a communication packet.

12. The variable width memory mapping method of Claim 8 wherein
 said information includes data associated with certain fields.

13. The variable width memory mapping method of Claim 12 wherein
 bits included in said data associated with certain fields are sequentially
 located within said memory cell.

14. The variable width memory mapping method of Claim 8 wherein a
 information storage system with a computer readable medium stores
 information in accordance with said variable width memory mapping
 process.

15. A variable memory width assignment method comprising:
 analyzing a data block configuration specification;
 identifying bits in a portion of said block of data, wherein said portion
 corresponds to information grouped in an arrangement that facilitates
 reduction of processing instructions; and

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assigning a memory location a width equal to said number of bits in said portion of said block of data.

16. The variable memory width assignment method of Claim 15 wherein said memory location is one of a plurality of memory locations of various widths.

17. The variable memory width assignment method of Claim 15 wherein said memory location has a unique identifying address.

18. The variable memory width assignment method of Claim 15 further comprises providing an association between said memory location and an external identifier.

19. The variable memory width assignment method of Claim 15 wherein said bits in said portion of said data block are arranged in a contiguous manner.

20. The variable memory width assignment method of Claim 15 wherein said data block is arranged in accordance with a communications packet configuration specification.

21. A variable width memory assignment system comprising:
a means for communicating memory location identifiers;
a means for storing information in a uniquely identifiable different width memory locations corresponding to said memory location identifiers;
and

a means for managing a connection with said uniquely identifiable different width memory locations.

22. The variable width memory assignment system of Claim 21 wherein said means for managing said connection supervises writing and reading of information to and from said uniquely identifiable different width memory locations.

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23. The process for variable register size assignment of Claim 22 wherein
 said means for storing said information returns a number of bits equal to
 the width of one of said uniquely identifiable different width memory
 5 locations in response to a read request.

24. The variable width memory assignment system of Claim 21 wherein
 said means for managing said connection includes a means for tracking a
 correspondence between said uniquely identifiable variable memory widths
 10 and register identifiers.

25. The variable width memory assignment system of Claim 24 wherein
 said register identifiers are provided by a means for processing said
 information.

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